NPA-0™ Access Network Processor

Integrated Traffic Management and Host CPU Core


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HIGHLIGHTS

- Single-chip, programmable, wire-speed network processor with 5-Gigabit aggregate throughput
- Flexible processing with programmable packet parsing, classifying, modifying and forwarding enabled through integrated Task Optimized Processors (TOPs)
- Integrated 5-Gigabit traffic management with hierarchical scheduling, supporting services defined by the Metro Ethernet Forum, e.g. MEF9 and MEF15
- On-chip Fabric Interface Controller (FIC) functionality for direct interfacing to Ethernet fabrics enabling system-wide traffic management
- Integrated hardware implemented search engines
- Integrated memory for lookup structures, statistics counters and TM control structures. Optional extension to external DRAM.
- Integrated TCAM for on-chip ACL processing
- On-chip OAM protocol processing offload
- On-chip IEEE1588v2 clock sync processing
- Synchronous Ethernet support, ITU-T G.8261
- On-chip MIPS34Kc core 650MHz for system control
- Supports oversubscription beyond 5-Gigabit processing throughput by smart classification and handling of up to 10Gbps
- Scaled-down version of Mellanox's NPA-1™ network processor targeting Ethernet access applications
  - Software compatible with Mellanox's NPA-2, NPA-3, NP-2®, NP-3® and NP-4 network processors

PACKAGE / PROCESS / POWER

- Package: FCBGA 484 pins, 23x23 mm, 1.00 mm pitch
- Process: TSMC 65nm
- Power dissipation: 5W typical
- Industrial operating temperature range: -40C° to 85C° ambient

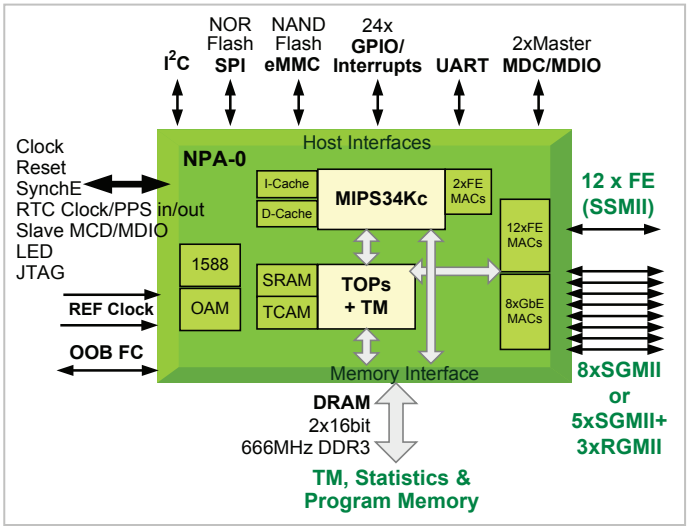
TARGET APPLICATIONS

- Line card, service card and pizza box applications
  - Fiber and copper Ethernet access switches
  - Ethernet demarcation devices
  - Wireless backhaul and base station aggregation (3G/4G and WiMax)
  - Copper access (DSLAMs)
  - Optical access (GPON/EPON OLTs and ONUs)
- Programming delivers a variety of applications such as L2 switching, Q-in-Q, MAC-in-MAC, PBB-TE, PBT, T-MPLS, MPLS-TP, VPLS, MPLS and IPv4/IPv6 routing

NETWORK I/Os

- 8 x 1-Gigabit Ethernet ports (SGMII/SERDES)
  - 3 ports can be RGMII
- SGMII interfaces support 2.5GE, 3.125Gbps SERDES for GPON
- 12 x Fast-Ethernet ports with SMII interfaces
  - Alternatively 4xSMII + 2xMII, or 8xSMII + 1xMII

Figure 1. Interfaces Diagram



† For illustration only. Actual products may vary.

DETAILED FEATURE LIST

Integrated Traffic Management

- 5-Gigabit traffic manager providing queuing and scheduling on all transmitted traffic on all ports
- Per Flow Queuing (PFQ) with 4 level hierarchical scheduling:
  - 32 ports/channels
  - 256 sub-ports
  - 1K classes/subscribers
  - 4K flow queues
- Policing: Per-flow metering, marking and policing
- Hierarchical WRED
- Shaping: Single and Dual leaky bucket controlling committed/peak rate/bursts (CIR, CIB, PIR, PIB) with IFG (Inter Frame Gap) emulation for accurate rate control
- Scheduling: WFQ and priority scheduling at each hierarchical level
- Work conserving and non-work conserving schedulers
- Frame size from 1 byte to 16K bytes
- Up to 1M frame buffers in external DRAM
- Per-frame timestamp and timeout drop
- Dynamic hitless reconfiguration and resource allocation
- OOB flow control and status interface
  - Elaborated congestion status reports
- Out-of-band flow control per physical port (1GbE or Fast Ethernet) or logical channel (TM level entity)
- Internal buffering and TM external buffering congestion status reporting via OOB signaling

NPU Programming

- Single-image programming model with no parallel programming or multi-threading
- Automatic allocation of frames to processing engines (TOPs)
- SW messages between TOP stages
- Automatic ordering of frames
- In-service software updates
- Large code space memory for multiple and complex applications
- Microcode compatible with Mellanox's NPA-2, NPA-3, NP-2, NP-3 and NP-4 network processors

Integrated Search Engines

- Performs flexibly defined lookups in switching, routing, classification and policy tables
- Programmable size and contents of search keys and results (associated information) per table
- Support for long keys and long results per table entry
- Table entries stored in integrated memory for fastest lookup time
- Tables may be stored in external DRAM memory
- On-chip state learning and updates of millions of addresses, sessions and flows per second

External Memory

- One interface with two controllers sharing the address and control buses, 2 x 16bit 666 MHz DDR3 DRAM
- Used for TM data & control, external lookup structures, external statistics and MIPS CPU memory
- Flexible bandwidth allocation for various tasks

Statistics and Counters

- Stored in integrated memory (shared with lookup structures) and/or in external DRAM
- Per-flow statistics for programmable events, traffic metering, policing and shaping
- Programmable threshold settings and threshold exceeded notification
- Dynamic allocation and auto association between counters and flows. Counters are automatically recycled when a flow is deleted or aged.
- Hardware implementation of token bucket per flow (srTCM, trTCM or MEF5)

Embedded CPU Core

- 650 MHz MIPS34Kc RISC with 9 stage execution pipeline. MIPS 16e Code Compression
- Power-down mode (WAIT)
- Bootable from ROM/NOR-flash via Serial Peripheral Interface or eMMC
- I^2C (Master/Slave) and MDC/MDIO (Master) serial management interfaces
- UART for management console

OAM Hardware Offload

- Per OAM session state tracking and reporting
- 802.1ag, 802.3ah and ITU-T Y.1731 compliant OAM offload
- Dedicated timer hardware blocks
  - KeepAlive (CCM) frame generation (as fast as 3.3ms) for precise and accurate session maintenance operations
  - KeepAlive watchdog timers for fastest detection
- LBM/LBR Message generation and detection
- LTM/LTR Message generation and detection
- Flexible statistics collection on a per session basis

Integrated FIC Functionality

- For architectures that adapt standard Ethernet switches as the switching fabric solution, the NPA-0™ integrates the FIC functionality
- Allows use of standard low-cost Ethernet switches as the backplane switch fabric
- Direct connection from NPA-0 on the line card to the backplane Ethernet switch
- Provides for system-wide QoS with per COS and per-flow congestion management

Sync Ethernet

- Enables on-board clock generation schemes using an external or recovered clock reference
- Provides output clock selection from each Serdes lane recovered clock

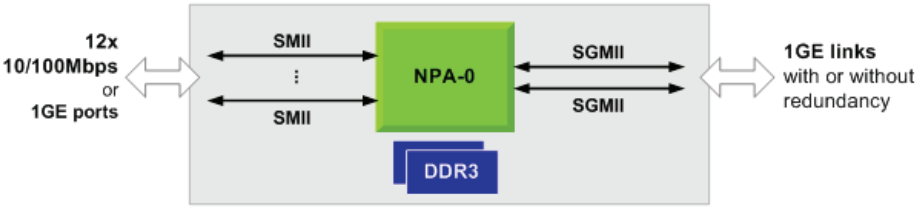
IEEE1588v2

- On-chip IEEE1588v2 clock sync processing offload for precise time synchronization among remote nodes and switches
- Can operate as ordinary clock, boundary clock, transparent clock, or a combination thereof
- Provides an accurate RTC, adjustable from the control CPU or an external source, and provides input and output timestamping for time and delay measurement
- HW assisted two-step IEEE1588v2 protocol

SYSTEM CONFIGURATIONS

NPA-0's flexibility and integration allows system vendors to deliver cost effective solutions that can easily adapt to changing market requirements. Illustrated below are several sample solutions.

Figure 2. Access switch or 1GE inter-carrier demarcation box (NNI)



In the following applications, NPA-0 provides switching and QoS to Radio and DSL line cards, and uplinks to aggregation networks:

Figure 3. Wireless backhaul aggregation switch

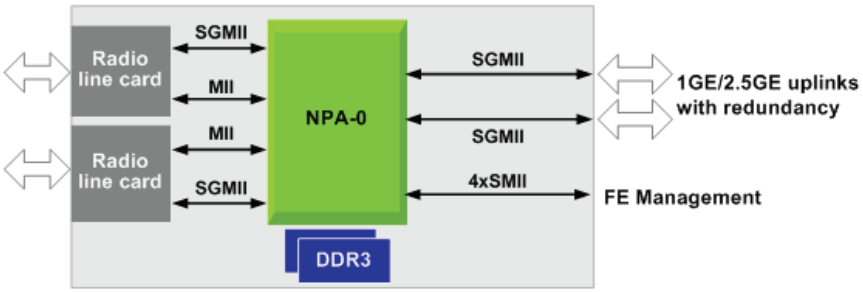
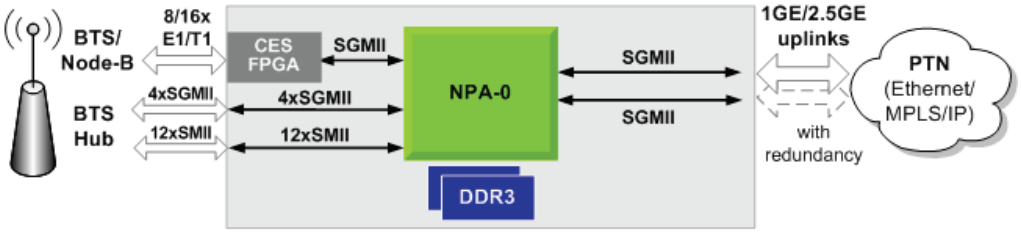


Figure 4. Wireless backhaul CES gateway



In the following application, NPA-0 provides switching and QoS to EPON/GPON links, and uplinks to aggregation networks:

Figure 5. EPON/GPON OLT

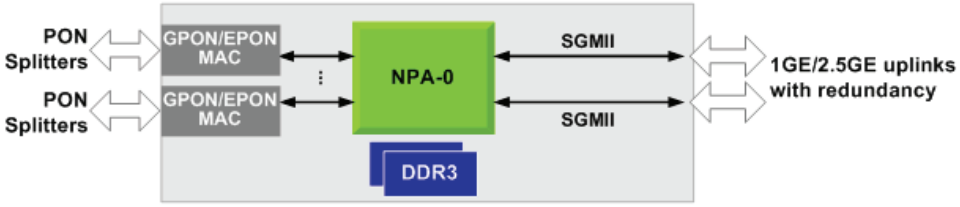


Table 1 - Part Number and Description

OPN	Description
20782902	NPA-0 Access Network Processor; RoHS compliant

350 Oakmead Parkway, Suite 100, Sunnyvale, CA 94085
Tel: 408-970-3400 • Fax: 408-970-3403
www.mellanox.com

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