MULTICORE PROCESSOR

PRODUCT BRIEF

TILE-Gx36 Processor

Thirty Six Core Processor SoC with 4x 10Gb Ethernet Ports, PCIe and Networking Offloads

The TILE-Gx36™ processor is optimized for networking and multimedia applications and delivers enormous computing power and I/O with complete "system-on-a-chip" features. The device includes 36 identical processor cores (tiles) interconnected with Mellanox's iMesh™ on-chip network. Each tile consists of a full-featured 64-bit processor core as well as L1 and L2 cache and a nonblocking Terabit/sec switch that connects the tiles to the mesh and provides full cache coherence among all the cores. The TILE-Gx36 is ideal for sophisticated networking applications requiring 20 to 40 Gbps of performance, as well as high-performance computing offload and high-density video transcoding workloads.

Powerful Processor Cores

- 36 cores at frequencies up to 1.2 GHz
- 64-bit architecture (datapath and address)
- Three execution pipelines
- Robust virtual memory system with TLBs, multiple page size support, and Hardwall™ protection
- Instruction Set Architecture (ISA) extensions for multimedia and SIMD processing

Cache

- 12 Mbytes total on-chip cache
- Dynamic Distributed Cache (DDC™) scalable hardware coherence
- 32 KB L1i, 32K L1d per core
- 256 KB L2 per core
- 9 MB coherent L3 cache cache per core

iMesh Interconnect

- Five independent low-latency mesh networks
- 60 Tbps aggregate bandwidth
- Non-blocking, cuthrough switching with 1 clock cycle per hop

APPLICATIONS

The TILE-Gx36 is ideal for applications such as:

- 40 Gbps of networking and security dataplane offload
- 40 Gbps packet filtering and bandwidth
- management
- 40 Gbps SSL/IPsec security protocol processing
- H.264/H.265 high-density video transcoding

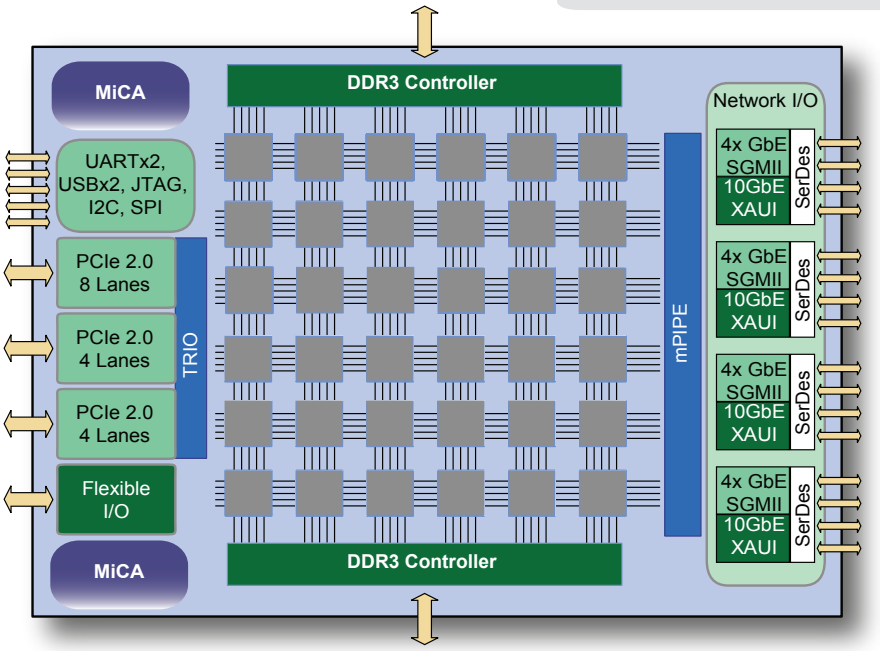

Figure 1: *TILE-Gx8036 Processor Block Diagram*

SPECIFICATIONS

PCI EXPRESS

- Three integrated Gen2 PCIe controllers (5G SerDes)
- Each configurable as root complex or endpoint
- High-performance coherent transaction DMA engine
- Multiple configurable transaction modes for efficient data movement
- SR-IOV support

STREAMIO INTERFACES

- Three high-performance transaction ports for chip-to-chip or FPGA interconnect
- Multiplexed with PCIe SerDes
- 20 Gbps peak performance per 4-lane port

INTEGRATED MEMORY CONTROLLERS

- Two 72-bit DDR3 controllers with ECC support
- 512 GB total memory capacity
- Up to 1,866 MTps speeds
- Advanced request reordering

NETWORKING INTERFACES

- Four 10 Gbps XAUI ports, including 20Gbps double-XAUI support
- Up to sixteen 10/100/1000 SGMII ports (multiplexed with XAUI ports)
- Egress QoS queuing and traffic shaping support
- IEEE1588v2 precision timing controller support
- IEEE802.1Qbb priority flow control and datacenter Ethernet (DCE) support

mPIPE™ WIRE-SPEED PACKET ENGINE

- C-programmable classification
- 40 Gbps aggregate throughput and 60 Mpps performance for minimum size packets
- Programmable checksum and CRC offload for packet headers and payload
- Multi-mode load-balancer with direct-to-cache packet delivery
- Flexible buffer manager with 32 configurable memory domains

CRYPTO AND COMPRESSION ACCELERATION

- MiCA™ engines deliver low-latency, high-bandwidth offload
- 40 Gbps encryption throughput (-E option)
- Support for IPsec, SSL, TLS, MACsec, SRTP, 3GPP
- Public Key accelerator (RSA, DSA, DH, ECC)
- True random number generator
- Deflate compress/decompress with Gzip compatibility

SYSTEM INTEGRATION FEATURES

- Two USB 2.0 interfaces; one host and one host/endpoint
- Four I2C interfaces
- One SPI (master) interface
- Two high-speed UART interfaces
- 64 GPIO/Interrupt pins
- JTAG port

PACKAGE INFORMATION

- 37.5 mm x 37.5 mm BGA
- 1 mm ball pitch device
- RoHS-6 compliant per EU 2002/95/EC

PACKAGE SIZE

- 1,265 BGA

Usage Examples

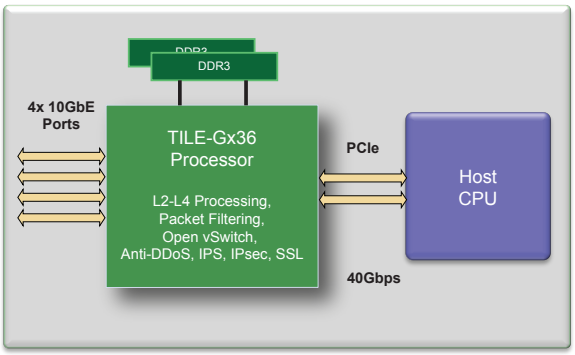

Figure 2. *High I/O "Front End" Application Processor*

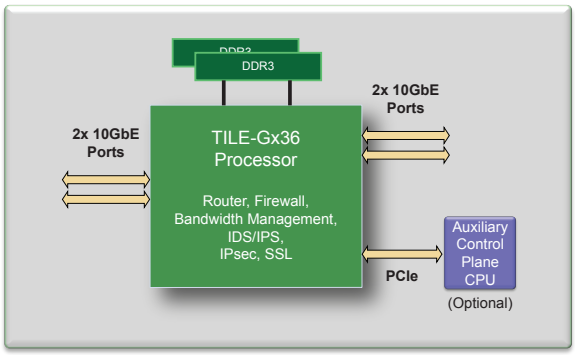

Figure 3. *40Gbps In-Line Dataplane Processor*

Ordering Part Number	Device	Max. Core Frequency	Max. Memory Speed	# of Cores	MiCA Accelerator	Typical Power*
TLR4-03680CH-10C-A3c	TILE-Gx36	1.0 GHz	1,600 MT/s	36	No	23 W
TLR4-03680CH-12C-A3c	TILE-Gx36	1.2 GHz	1,866 MT/s	36	No	28 W
TLR4-03680CH-10CE-A3c	TILE-Gx36	1.0 GHz	1,600 MT/s	36	Yes	25 W
TLR4-03680CH-12CE-A3c	TILE-Gx36	1.2 GHz	1,866 MT/s	36	Yes	31 W

* Power may vary based on application and I/O configuration.

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